WHAT IS CLAIMED IS:

1. A digital to analog converter architecture comprising:

an input circuit for M+1 levels representing a signal value;

a matching element array having a range of 2M bits connected to the input circuit;

a dynamic element matching logic for 2M bits controlling the matching element array responsive to the signal value; and

an output circuit receiving an output from the matching element array.

2. A digital to analog converter architecture as previously defined in claim 1 wherein the input circuit comprises a digital input of M+1 levels connected to a thermometer decode.

3. A digital to analog converter architecture comprising:

an input circuit for X bits representing a signal value, the X bits including M most significant bits;

a matching element array having a range of 2M bits connected to the input circuit;

a dynamic element matching logic for 2M bits controlling the matching element array responsive to the signal value; and

an output circuit receiving an output from the matching element array.

4. A digital to analog converter architecture as previously defined in 3 wherein the digital input of M bits is connected to a thermometer decode.

5. A digital to analog converter architecture comprising:

an input circuit for X bits representing a signal value, the X bits including M most significant bits (MSBs) and N least significant bits (LSBs);

a first matching element array having a range of 2M bits connected to the input circuit;

a first dynamic element matching logic for 2M bits controlling the matching element array responsive to the value of the MSBs;

a second matching element array having a range of 2N bits connected to the input circuit;

a second dynamic element matching logic for 2N bits controlling the matching element array responsive to the value of the LSBs; and

an output circuit receiving an output from the first and second matching element arrays.